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PATENT
Customer No. 22,852
Attorney Docket No. 6720.0068

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Shih-Chiang TSAO et al.	Group Art Unit: 2661
Application No.: 09/955,296	Examiner: Unknown
Filed: September 19, 2001	
For: METHOD AND APPARATUS FOR SCHEDULING PACKET-SWITCHED NETWORKS	Confirmation No.: 8161

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents listed on the attached PTO 1449. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application.

Copies of the listed documents are attached.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the

documents as prior art against any claim in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the U.S. Patent and Trademark Office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: April 22, 2004

By: _____
Richard V. Burgujian
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OMB No. 0651-0031

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Technology Center 2600

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	6720.0068	Appln. No.	09/955,296
Applicant	Shih-Chiang TSAO et al.		
Filing Date	September 19, 2001	Group: 2661	Examiner: Unknown

	OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)
	A. K. Parekh et al., "A generalized processor sharing approach to flow control in integrated services networks: the single-node case," *IEEE/ACM Trans. Networking*, pp. 344-357, June 1993
	J. C. R. Bennett et al., "WF^2Q: Worst-case fair weighted fair queueing," *Proc. IEEE INFOCOM '96,* pp. 120-128, San Francisco, CA, March 1996.
	S. J. Golestani, "A self-clocked fair queueing scheme for broadband applications," *Proc. INFOCOM '94*, pp 636-646, June 1994.
	L. Zhang, "Virtual Clock: A new traffic control algorithm for packet-switched networks," *ACM Trans. on Computer Systems*, vol. 9, no. 2, pp. 101-124, May 1991.
	M. Shreedhar et al., "Efficient fair queuing using deficit round-robin," *IEEE/ACM Trans. Networking*, vol. 4, no. 3, pp. 375-385, June 1996.
	D. Stiliadis et al., "Efficient fair queueing algorithms for packet-switched networks," *IEEE/ACM Trans. Networking,* vol. 6, no. 2, pp. 175-185, April 1998.
	S. Suri, et al. "Leap forward virtual clock: a new fair queuing scheme with guaranteed delays and throughput fairness," P*roc. INFOCOM '97,* pp. 557-565, April 1997.
	D. Stiliadis et al., "Latency-rate servers: a general model for analysis of traffic scheduling algorithms," *IEEE/ACM Trans. Networking,* vol. 6, no. 5, pp. 611-624, Oct. 1998.
	N. Matsufuru et al. "Efficient fair queueing for ATM networks using uniform round robin," *Proc. INFOCOM '99,* pp. 389-397, March 1999.
	M. Katevenis et al., "Weighted round-robin cell multiplexing in a general-purpose ATM switch chip," *IEEE Journal on Selected Areas in Communication,* vol. 9, no. 8, pp. 1265-79, October 1991.
	H. M. Chaskar et al., "Fair scheduling with tunable latency: A Round Robin approach," *IEEE Globecom '99*, pp. 1328-1333, December 1999.
	J. C. R. Bennett et al., "High speed, scalable, and accurate implementation of packet fair queueing algorithms in ATM networks," *Proc. ICNP '97,* pp. 7-14, Oct. 1997.
	V. Nageshwara Rao et al., "Concurrent access of priority queues," *IEEE Trans. on Computers,* vol. 37, no. 12, pp. 1657-1665, Dec. 1988.
	J. L. Rexford et al., "Hardware-efficient fair queueing architectures for high-speed networks," *Proc. INFOCOM* '96, pp. 638-646, March 1996.

Examiner	Date Considered

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO 1449 — Patent and Trademark Office - U.S. Department of Commerce